# TRACE-PAD INTERFACE FOR IMPROVED SIGNAL QUALITY

This application is a continuation of US Patent Application No. 08/951,556, filed October 16, 1997, which is incorporated herein by reference.

## Field of Invention

The invention relates generally to an interconnect structure for use in the construction of a printed circuit or wire board. More specifically, the invention relates to an improved interconnection interface between a relatively thin signal trace and a relatively wide component pad on the surface of a printed wire board in order to better accommodate high speed signals which are conducted along or through such an interface.

## Background of Invention

Integrated circuit devices and other types of electronic components, such as component 7 in Fig. 1A, having multiple pinouts or leads 5 are often mounted onto the surface of a printed wire board 14 such that each pin or lead 5 of the electronic component 7 is mounted or soldered to a typically rectangularly-shaped deposit of copper (i.e. "pad" 12) present on the surface of the printed wire board 14. (The means for mounting electronic components directly onto the surface or a printed wiring board is commonly referred to as "surface mount technology".) The many component pads 12 which typically exist on the surface of the printed wiring board 14 are interconnected together in a predetermined configuration by thin copper signal lines (i.e. "traces" 10). Conventionally, as is shown in Fig. 1, the practice in the industry has been to lay out a signal trace 10 so that it intersects one of the sides of the pad 12 at approximately the middle thereof. Typically too,

the layout practice dictates that the trace 10 be orientated to intersect the side of the pad at a substantially ninety degree angle as shown.

Referring to fig. 1B, 4S
As the internal operating speed of integrated circuits (IC's) such a microprocessors and memories increase with improving semiconductor process technology, the digital signals 17 which travel along the printed circuit board 14 between the various components 7 thereof also have to reach their destinations 19, i.e. trigger their input receivers, more quickly in order to take advantage of the increased IC operating speed. For example, as shown in fig. 1C, in order to decrease memory access time in a computer, the control signals 42 produced by a memory controller 40 must reach the memory 64 more quickly and at a greater frequency.

Fig. 2A shows a typical digital binary signal 15 which goes from a low, or binary 0, state to a high, or binary 1, state. Since the transition of the signal from the low state to the high state or vice versa cannot be accomplished instantaneously, there exists a rise time $t_r$ and a fall time $t_f$ which respectively results in a sloping leading edge 16 and a sloping trailing edge 18. In order to make a control signal reach or trigger an input receiver faster, it is necessary to (a) minimize the rise and/or fall time, and (b) increase the frequency at which control signals are sent. In the present art, the rise/fall time has fallen to below one nanosecond, with signal frequency at 66 MHz.

Fig. 2B shows the binary digital signal 15 represented in the frequency domain. It will be noted that each frequency component $i$ of the digital signal has a voltage $v_o(i)$ associated therewith (phase information is not shown in Fig. 2B).

On a printed circuit board, the junction between a signal trace and a component pad, such as the prior art interface shown in Fig. 1, represents an impedance discontinuity since (a) the width of the conducting path suddenly drastically increases at the pad and (b) the cross-sectional area or thickness of the conducting path increases due to solder present on the pad. When a digital signal such as that shown in Figs. 2A and 2B travels across an impedance discontinuity, the voltage or power of the signal is split at the trace/pad junction so that a portion $v_o(i)/x_1(i)$ of each frequency component $i$ of the signal travels back in the opposite direction of the wave front. The remaining portion $v_o(i)/x_2(i)$ of each frequency component $i$ of the signal travels in the original or forward direction. The values $x_1(i)$ and $x_2(i)$ are greater than or equal to one. The greater the ratio of the larger impedance to the smaller impedance at the discontinuity, the more the voltage of the signal components will be affected by the discontinuity, i.e., the smaller the value of $x_1(i)$.

The portions $v_0(i)/x_1(i)$ of each frequency component of the signal which travel in the opposite direction will similarly reflect at the next impedance discontinuity in their path, and the same will happen to the frequency components $v_o(i)/x_2(i)$ which travel in the forward direction. The reflected portions of the signal will recombine with the wavefront and modify its appearance. In the frequency domain, this will be visible as a change in voltage associated

with each frequency component. In the time domain, this will appear as one or more "glitches" or "inflection points". An example of one such glitch caused by a single discontinuity is shown in idealized form in the time domain diagram of Fig. 3 where at time/position $t_o$ the forward portion $\sum v_o(i)/x_2(i)$ of the signal travels across the impedance discontinuity presented by the prior art trace/pad junction and a short time $t_1$ later the reflected and rebounded portion $\sum v_o(i)/x_1(i)$ of the signal recombines.

The physical size of electronic components mounted on a printed circuit board means that the components have to be distributed across the board in such a way that relatively long signal traces cannot be avoided. Inflection points or glitches on the signal will be produced by the impedance discontinuities along the conduction path the signal travels. These non-monotonic wave forms appear as multiple rising (or falling) edges where only one rising (or falling) edge was desired. One or a combination of the glitches or inflection points may produce false triggers at input receivers. The invention seeks to reduce the tendency of this phenomenon.

Summary of Invention

In a broad sense, the invention provides an interconnect structure for connecting together a relatively narrow printed wire board signal trace and a substantially wider component pad in a manner which reduces the amount of signal reflection at the trace/pad junction. The reduced signal reflection thus reduces the tendency to produce false triggers at

input receivers. This objective is accomplished by routing or laying out a given signal trace so that it is electrically connected to a corner of the substantially rectangularly shaped pad, such that a longitudinal centerline axis of the trace will form an angle in the range of 110 to 160 degrees, and preferably approximately 135 degrees, with a proximate side of the component pad. This topology results in a gradual increase in the width of the conducting path thereby reducing the impedance mismatch between the signal trace and the component pad. The above described signal layout practice provides the advantage of not adversely affecting the manufacture of a printed circuit board, particularly the process of reflow soldering, as explained in greater detail below.

According to one aspect of the invention, there is provided a method of improving the transmission quality of a digital signal on a printed wire board wherein the digital signal travels along a conduction path comprising a relatively narrow signal trace which interfaces with a substantially wider, substantially rectangularly shaped component pad having at least one corner. The method includes the step of electrically connecting the signal trace to the corner of the substantially rectangular pad such that a longitudinal centerline axis through the signal trace forms an angle of approximately 135 degrees to a proximate side of the component pad.

According to another aspect of the invention, there is provided a method for improving the signal transmission quality of a printed wire board comprising relatively narrow signal traces electrically connected to substantially wider component pads of substantially

rectangular shape having at least one corner. The method comprises the step of routing or laying out the signal traces such that the longitudinal centerline axis through each such trace is respectively electrically connected to the corners of the substantially rectangular pads to form angles of approximately 135 degrees to proximate sides of the respective pads.

Other details of the invention will become more apparent from the following detailed description and drawings wherein like reference numerals depict like elements.

Brief Description of Drawings

Fig. 1 is a diagram illustrating a typical junction between a printed wire board signal trace and a component pad as conventionally laid out in the prior art;

Fig. 2A is a diagram of a portion of a binary digital signal as represented in the time domain;

Fig. 2B is a diagram of the signal shown in Fig. 2A as represented in the frequency domain;

Fig. 3 is an idealized diagram of a portion of a noisy digital signal in the time domain which features multiple rising edges caused by an impedance discontinuity at the junction between a trace and a pad;

Fig. 4 is a diagram illustrating an interface between a printed wire board signal trace and a component pad in accordance with a preferred embodiment of the invention;

Fig. 4A is a schematic diagram of the interface of Fig. 4, shown in cross-section;

Fig. 5 is a diagram of the junction of Fig. 4 illustrating a gradually increasing conductive path width;

Fig. 6 is a diagram illustrating an interface between two signal traces and a component pad in accordance with a preferred embodiment of the invention;

Fig. 7 is a block diagram of a memory system;

Fig. 8 is an illustration of one example of a portion of a mass produced printed wire board constructed in accordance with the principles of the invention.

Detailed Description of Preferred Embodiments

Fig. 4 illustrates an interconnect structure 20 for connecting together a relatively narrow printed wire board signal trace 22 and a substantially wider, substantially rectangular, component pad 24 in accordance with the preferred embodiment of the invention. The trace 22 has a width $w_t$ of about 4 mils (thousands of an inch) and pad 24 has a width $w_p$ of about 22 mils. The trace 22 has a cross-section or thickness $t_t$ of about 1.2 mils, and, due partially to the solder typically placed on the pad 24 for mounting the IC component pin, the pad 24 has a cross-section or thickness $t_p$ in the range of about 6 to 7 mils. These dimensions are typical of the present art. However, unlike the prior art, it will be noted that trace 22 is electrically connected to a corner 28 of substantially rectangular pad 24 and routed or laid out such that a longitudinal centerline axis of the trace 22 forms an angle $\theta$ in the range of about 110 to 160 degrees with proximate side 26b of the pad 24, with the most preferred angle $\theta$ being about 135 degrees.

As illustrated in Figs. 4 and 5, the topology of interconnect structure 20 permits a gradual increase in the width of the electrically conductive path between the signal trace 22 and component pin or lead (not shown). The gradual increase results in smaller impedance changes or graduations along the conductive path (as represented in Fig. 5) compared to the prior art interconnect structure topology shown in Fig. 1. Reflections will still occur, but since the reflection coefficient R at any given frequency ω is related to the ratio of the change in impedance Z at the boundary, i.e.,

$$R(\omega) = \frac{Z_2(\omega) - Z_1(\omega)}{Z_2(\omega) + Z_1(\omega)},$$

where $Z_1$ is the impedance at the near side of the boundary and $Z_2$ is the impedance at the far side of the boundary, the signal crossing from the near side to the far side of the boundary, the reflections will be smaller in amplitude as compared to the prior art trace/pad interface shown in Fig.1.

The invention is preferably utilized in circumstances where the signal trace is sufficiently long so as to act like a transmission line. This is generally believed to occur when the length of the signal trace is approximately at least 1/6th of the "transition electrical length" of the digital signal, i.e., the rise or fall time of the signal multiplied by the propagation speed of the signal along the signal trace (which is typically about 1/2 the speed of light for FR4 type board). The invention is particularly useful when the length of the

signal trace approaches or exceeds the transition electrical length of the digital signal since in such circumstances, assuming no other impedance discontinuities along the conduction path, reflections caused by the trace/pad interface have a greater likelihood of not recombining within the rise or fall time of the signal.

When it is desired to couple two signal traces to a component pad, it is preferred to connect the signal traces 22 to opposite corners of the substantially rectangularly shaped component pad as shown in Fig. 6. This will ensure the most gradual impedance gradient in the event a digital signal has to flow from trace 22a, through the pad 24, to trace 22b.

It may also be thought desirable to gradually increase or flare the width of the signal traces as they approach component pads on printed wire boards in order to further reduce the impedance graduations along the conductor path. However, this approach leads to two particular disadvantages which are not conducive to the mass manufacture of printed circuit boards. One such disadvantage relates to the wire density of the printed wire board; flaring or widening the signal traces means that the board will accommodate a lower density of signal traces, which is contrary to the continuing trend towards ever greater miniaturization. Another disadvantage relates to the process by which printed circuit boards are assembled using surface mount technology assembly techniques. The assembly process generally includes a reflow soldering stage wherein electronic components are soldered *en masse* to their respective component pads on the printed wire board. Flaring the ends of the signal traces effectively results in increasing the mass of the component pads which will then not be

able to accumulate enough heat in the conventional reflow soldering process to form a good joint with the associated component pins or leads. This condition is commonly termed a "cold solder joint" and results in printed circuit boards of poor signal transmission quality. In contrast, the preferred embodiment of the invention described above does not interfere with the conventional reflow soldering process nor is the wire or trace density of the printed wire board unduly compromised.

The assignee of the instant application has developed a mass production printed circuit dual-in-line-memory-module (DIMM) utilizing the design layout principles of the invention. Fig. 7 shows a block diagram of a memory system 38 which employs the DIMM. The system 38 comprises a memory controller 40 which controls the flow of thirty three bit Control 42 , seventy two bit Data 44, and twelve bit Address 46 signals to each of a plurality of DRAM DIMM slots 48. A processor, not shown, sends the Data 44 and Address 46 lines to the memory controller 40. Each of the DIMM slots 48 is a hardware connector into which DRAM DIMMs can be inserted. The system 38 is designed such that the controller 40 resides on one printed circuit board while the DRAM DIMMS reside on another circuit board. The system 38 utilizes digital signals having a rise/fall time of below 1 nanosecond and the maximum frequency of the Control signals 42 is up to 66 MHz. Using a commercially available simulation software package ("simulator"), it was noted that the DIMM, as notionally assembled onto a conventionally laid out printed circuit board, occasionally exhibited errant behaviour due to false triggering of the DIMM memory. However, when the

DIMM was modelled using a printed wire board 43 wherein certain signal traces 22 carrying critical control signals 42 were connected to the corners of the pads 24 at 135 degree angles as described above, the simulator showed that the preferred embodiment of the invention improved upon the errant behaviour of the originally modelled DIMM memory 47. Fig. 8 shows an example of a portion of one surface of such a DIMM printed circuit board 43 which was constructed and mass produced.

Those skilled in the art will appreciate that other modifications and variations may be made to the preferred embodiments disclosed herein whilst keeping within the spirit and scope of the invention as defined by the claims which follow: